HXRHPPC Processor
Rad Hard Microprocessor

Honeywell

The monolithic, radiation hardened HXRHPPC processor is fabricated with Honeywell's 0.35µm silicon-on-insulator CMOS (SOI-V) technology and is based on and compatible with Freescale's PowerPC 603e™ processor. It is designed for use in radiation sensitive environments. The HXRHPPC processor operates over the full military temperature range and requires a supply voltage of 3.3V ± 0.3V.

Honeywell's SOI-V technology is radiation hardened through the use of advanced and proprietary design, layout and process hardening techniques.

The HXRHPPC processor is a low-power, reduced instruction set computing (RISC) microprocessor. It implements the 32-bit portion of the PowerPC architecture, which supports 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating point data types of 32 and 64 bits.

The HXRHPPC processor is a superscalar processor capable of issuing and completing as many as two instructions per cycle and can complete a branch. This combined with four software controllable power-saving modes makes it a highly efficient, low power device.

Applications include on-board spacecraft control and payload control.

The HXRHPPC processor can be ordered under the SMD drawing 5962-07A01.

FEATURES

- Fabricated on SOI-V Silicon On Insulator (SOI) CMOS - 350 nm, 4 level metal Process
- Core frequency up to 80 MHz
- Programmable integrated PLL
- Power Supply = 3.3 V ± 0.3 V
- Power Dissipation: 7.6W max, 3.6V, 125°C, (GCLK=80 MHz, SYSCLK=20MHz)
- Operating Temp Range is -55°C to +125°C
- Packages
  - 240 Ceramic Quad Flat Pack
  - 255 Ceramic Ball Grid Array
  - 255 Ceramic Land Grid Array
- Radiation Performance
  - Total Ionizing Dose: >300krad(Si)
  - Soft Error Rate: $<1.5 \times 10^{-5}$ Upsets/processor-day
- High-performance, superscalar microprocessor
  - Up to two instructions issued and completed per clock plus a branch execution
  - Up to five instructions in execution per cycle.
  - Single cycle throughput for most instructions
- Five independent execution units and two register files
  - Branch Processing Unit (BPU) for static branch prediction
  - Integer Unit with 32 32-bit General Purpose Registers (GPR)
  - Fully IEEE 754-compliant Floating Point Unit (FPU) with 32 32-bit Floating Point Registers (FPR), supports both single and double precision operation
  - Load Store Unit (LSU) for data transfer between data cache and GPRs and FPRs
  - System Register Unit (SRU) that executes condition register (CR), special-purpose register (SPR) instructions, and integer add/compare instructions
- High Instruction and Data throughput
  - Zero-cycle branch capability (branch folding)
  - Programmable static branch prediction on unresolved conditional branches
  - Instruction fetch unit capable of fetching two instructions per clock from the instruction cache
  - A six-entry instruction queue that provides lookahead capability
  - Independent pipelines with feed-forwarding that reduces data dependencies in hardware
  - 16-Kbyte data cache and 16-Kbyte instruction cache, 4-way set-associative
  - Cache write-back or write-through operation programmable on a per page or per block basis
- Facilities for enhanced system performance
  - A 32- or 64-bit split-transaction external data bus with burst transfers
- Integrated power management
  - Internal processor/bus clock multiplier
  - Four power saving modes
  - Dynamic power management mode
- In-system testability and debugging features through JTAG boundary-scan capability

RADIATION HARDNESS RATINGS (1)

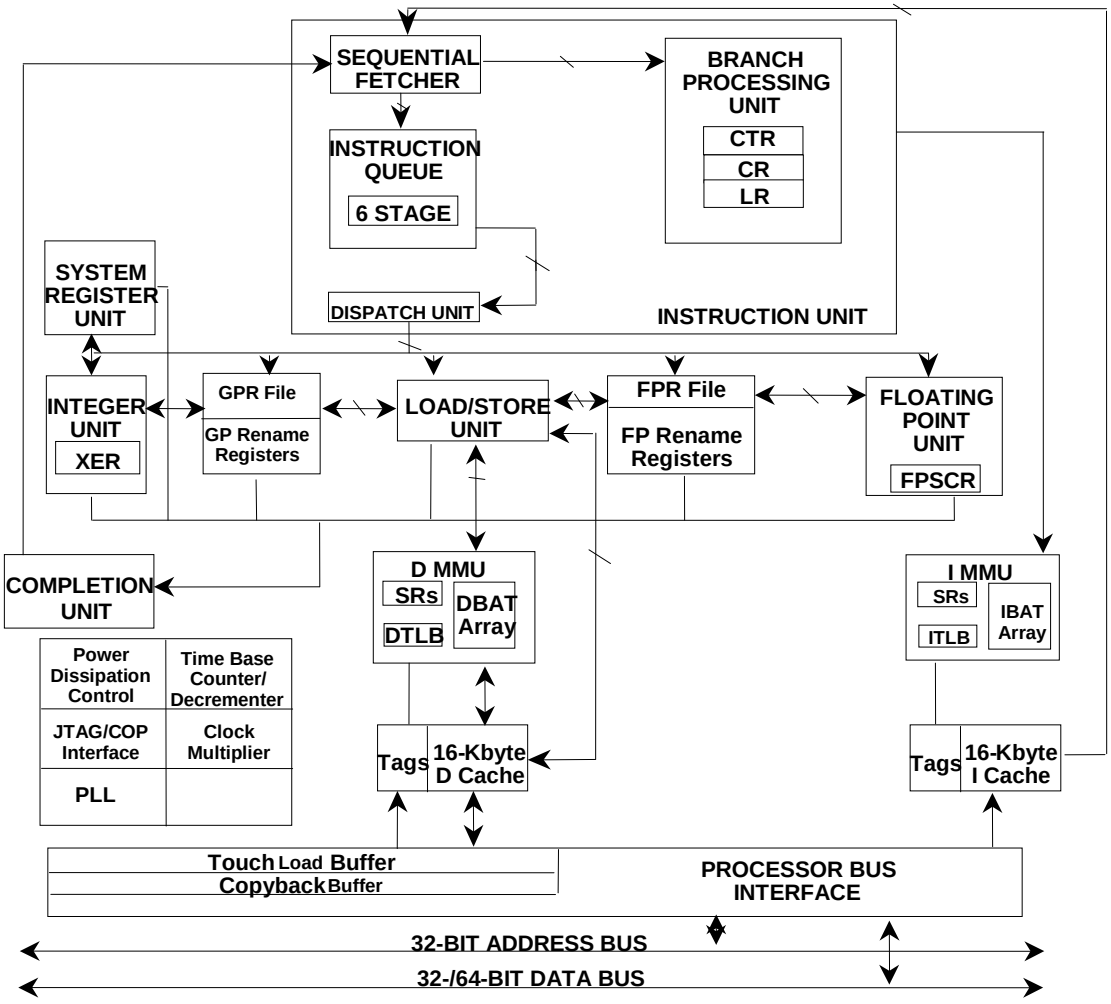
The combination of the SOI CMOS technology and circuit design makes this processor radiation hardened and immune to latchup.

Description	Specification	Description	Specification
Total Dose	$3x10^{5}$ rad(Si)	Dose Rate Upset	$5x10^{10}$ rad(Si)/s
Soft Error Rate	$\leq 1.5x10^{-5}$ Upsets/processor-day, GEO, AP8 min	Dose Rate Survivability	$1x10^{12}$ rad(Si)/s
Neutron Fluence	$1x10^{14}$ N/cm2		

Notes:

(1) Device will not latch up due to any of the specified radiation exposure conditions.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



HXRHPPC PROCESSOR

MICROPROCESSOR DESCRIPTION

The HXRHPPC processor integrates five execution units—an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU), and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high system efficiency and throughput. Most integer instructions have throughput of one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The processor provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). It also supports block address translation through the use of two independent instruction and data block address translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation.

The HXRHPPC processor has a selectable 32- or 64-bit external data bus and a 32-bit address bus. The interface protocol allows multiple masters to compete for system resources through a central external arbiter. There is a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches. The HXRHPPC processor supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O.

SIGNAL DEFINITIONS

The HXRHPPC processor provides the same signal IO and definitions as the Freescale 603e Microprocessor, except for the following signals. Reference SMD 5962-07A01 for pinout locations.

Signal Name	603e Signal	Definition
IN_LOCK	NC	De-asserted when the skew between the rising edge SYSCLK and falling edge C1_FDBK is greater than or equal to 1nsec. (NC on 240 pin CQFP package)
LOCK_DET	NC	Asserted when the phase of the rising edge of SYSCLK and the falling edge of C1_FDBK are consistently within 90 degrees, for 10 SYSCLK cycles. (NC on 240 pin CQFP package)
LOCK_OE	NC	Asserted will enable LOCK_DET and IN_LOCK outputs. (VSS on 240 pin CQFP package)
MSRIP	NC	Asserted indicates the MSR IP bit will initialize to 1 at HRESET, ref. Freescale™ Groucho Core Book IV, p.10, p.31; Freescale MPC603e™ User's Manual p.4-13. (VDD on 240 pin CQFP package)
PVR_SEL	NC	Asserted selects the Honeywell PVR value, de-asserted selects the original Freescale™ PVR value. (VSS on 240 pin CQFP package)
FREQ_SEL(0:1)	(NC:NC)	Configures the PLL for the frequency range of the phase detector. (FREQ_SEL(0) = VDD on 240 pin CQFP package)
PLL_CFG(0:4)	PLL_CFG(0:3)NC	Configures the PLL operation and the multiplier ratio. Contact Honeywell for programming selection table. (PLL_CFG(4) = VSS on 240 pin CQFP package)
WAITR	NC	Asserted will add additional non-overlap between C1 and C2 clocks. (VSS on 240 pin CQFP package) (NC on Freescale™ PPC)
VDD	OVDD	Supplied by VDD
VDD	AVDD	Supplied by VDD

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ABSOLUTE MAXIMUM RATINGS [1]

Symbol	Parameter	Ratings		Units
		Min	Max	
V_{DD}	Positive Supply Voltage (2)	-0.5	4.6	Volts
V_{IN}	Voltage on Any Input Pin (2)	-0.5	VDD + 0.5	Volts
V_{OUT}	Voltage on Any Output Pin (2)	-0.5	VDD + 0.5	Volts
I_{IN}	Average Input Current		±50	mA
I_{OUT}	Average Output Current		±50	mA
T_{STORE}	Storage Temperature (125 °C for CBGA)	-65	150	°C
T_{SOLDER}	Soldering Temperature (5 sec) (4)		270	°C
T_J	Junction Temperature		175	°C
P_{JC}	Package Thermal Resistance (Junction to Case) 240 pin		1.3	°C/W
P_{JC}	Package Thermal Resistance (Junction to Case) 255 pin		0.9	°C/W
V_{PROT}	ESD Voltage (Human Body Model)	2000		V

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS
(3) Not used
(4) Maximum soldering temp of 270°C can be maintained for no more than 5 seconds.

RECOMMENDED OPERATING CONDITIONS[1]

Symbol	Parameter	Limits			Units
		Min	Typ	Max	
V_{DD}	Positive Supply Voltage	3.0		3.6	Volts
V_{IH}	High Level Input Voltage	0.7 V_{DD}		V_{DD}	Volts
V_{IL}	Low Level Input Voltage	0.0 V_{DD}		0.3 V_{DD}	Volts
T_C	External Package Temperature	-55	25	+125	°C
V_{IN}	Voltage On Any Pin	-0.3		V_{DD}+0.3	Volts
SYSCLK	System Clock			50	MHz
GCLK	Core Clock			80	MHz

(1) Voltages referenced to Vss

ELECTRICAL AND TIMING SPECIFICATIONS

Please refer to the Freescale 603e™ datasheet for further functional details and the SMD drawing 5962-07A01 for electrical and timing details.

QUALITY AND RELIABILITY

The HXRHPPC processor is offered as QML qualified Class Q+ and Class V. For more than 15 years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems.

SOFTWARE TOOL SUPPORT

Because the HXRHPPC processor is derived from licensed commercial PowerPC 603e™ technology, it is compatible with all commercial 603e PowerPC™ software tools. Honeywell uses Wind River Systems' Tornado™ environment and the GNU C/C+ tools. Additionally, Honeywell can provide a Prototype/Software Development Unit (Ganymede) to support software debug.

PACKAGING

The processor is offered in three package types.

- 240 Ceramic Quad Flat Package
- 255 Ceramic Ball Grid Array
- 255 Ceramic Land Grid Array

These packages are constructed of multi-layer ceramic (Al_2O_3) and contain internal power and ground planes. The package lid material is Kovar.